1. A system for configuring and operating an adaptive circuit, the system comprising:

a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure and provide the first operand data to the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes, in response to the first configuration information, and the interconnection network further operative to reconfigure and provide the second operand data to the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes, in response to the second configuration information, the first functional mode being different than the second functional mode.

2. The system of claim 1, wherein the first executable information module provides a first system operating mode.

3. The system of claim 2, further comprising:

a second executable information module, the second executable information module providing a second system operating mode.

4. The system of claim 1, further comprising:

a memory coupled to the plurality of heterogeneous computational elements and to the interconnection network, the memory operative to store the first configuration information and the second configuration information.

5. The system of claim 1, wherein the first configuration information and the second configuration information are stored in a second plurality of heterogeneous computational elements configured for a memory functional mode.

6. The system of claim 1, wherein the first configuration information and the second configuration information are stored as a configuration of the plurality of heterogeneous computational elements.

7. The system of claim 1, wherein the first executable information module is stored in a machine-readable medium.

8. The system of claim 1, wherein the first executable information module is transmitted through an air interface.

9. The system of claim 1, wherein the first executable information module is transmitted through a wireline interface.

10. The system of claim 1, wherein the first executable information module is embodied as a plurality of discrete information data packets.

11. The system of claim 1, wherein the first executable information module is embodied as a stream of information data bits.

12. The system of claim 1, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of specific architectures, the plurality of specific architectures including functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, routing, control, input, output, and field programmability.

13. The system of claim 1, wherein the plurality of functional modes includes linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

14. The system of claim 1, further comprising:

a controller coupled to the plurality of heterogeneous computational elements and to the interconnection network, the controller operative to coordinate the configuration of the plurality of heterogeneous computational elements for the first functional mode with the first operand data and further coordinate the reconfiguration of the plurality of heterogeneous computational elements for the second functional mode with the second operand data.

15. The system of claim 1, further comprising:

a second plurality of heterogeneous computational elements coupled to the interconnection network, the second plurality of heterogeneous computational elements configured for a controller operating mode, the second plurality of heterogeneous computational elements operative to coordinate the configuration of the plurality of heterogeneous computational elements for the first functional mode with the first operand data and further coordinate the reconfiguration of the plurality of heterogeneous computational elements for the second functional mode with the second operand data.

16. The system of claim 1, wherein the system is embodied within a mobile station having a plurality of operating modes, the plurality of operating modes including mobile telecommunication, personal digital assistance, multimedia reception, mobile packet-based communication, and paging.

17. The system of claim 1, wherein the system is embodied within a server having a plurality of operating modes.

18. The system of claim 1, wherein the system is embodied within an adjunct network entity having a plurality of operating modes.

19. The system of claim 1, wherein the plurality of heterogeneous computational elements are configured to generate a request for a second executable information module, the second executable information module providing a second system operating mode.

20. The system of claim 1, wherein the system is embodied within an integrated circuit.

21. The system of claim 1, wherein the first executable information module further comprises:

a first routing sequence coupled to the first configuration information to provide routing of the first configuration information within the interconnection network; and

a second routing sequence coupled to the second configuration information to provide routing of the second configuration information within the interconnection network.

22. The system of claim 1, wherein the first executable information module further comprises:

a power control sequence to direct the interconnection network to not provide a clock signal to a selected heterogeneous computational element of the plurality of heterogeneous computational elements.

23. The system of claim 1, wherein the first executable information module further comprises:

an iteration control sequence to direct a temporal continuation of a selected configuration of the plurality of heterogeneous computational elements.

24. The system of claim 1, wherein the first configuration information is a reference to a previously stored configuration sequence.

25. The system of claim 1, wherein a first portion of the plurality of heterogeneous computational elements are operating in the first functional mode while a second portion of the plurality of heterogeneous computational elements are being configured for the second functional mode.

26. A system for operating an adaptive and reconfigurable integrated circuit, the system comprising:

means for providing a first configuration sequence to configure a plurality of heterogeneous computational elements to form a first computational unit for the performance of a first selected function;

means for providing a second configuration sequence to reconfigure the plurality of heterogeneous computational elements to form a second computational unit for the performance of a second selected function;

means for self-routing the first configuration sequence and the second configuration sequence;

means for providing first operand data to the first computational unit for the performance of the first selected function; and

means for providing second operand data to the second computational unit for the performance of the second selected function

27. The system of claim 26, further comprising:

means for coordinating timing of the configuration of the plurality of heterogeneous computational elements to precede reception of the first operand data to be utilized in the performance of the first selected function.

28. The system of claim 26, further comprising:

means for maintaining the configuration of the plurality of heterogeneous computational elements for a repetition of the performance of the first selected function.

29. The system of claim 26, further comprising:

means for inserting a configuration reference into a received data stream.

30. The system of claim 26, further comprising:

means for inserting a power control reference into a received data stream.

31. An executable information module for operating an adaptive system, the adaptive system including a plurality of computational elements having a corresponding plurality of fixed and differing architectures, the adaptive system further including an interconnect network responsive to configure the plurality of computational elements for a plurality of operating modes, the module comprising:

a plurality of information sequences;

wherein a first information sequence of the plurality of information sequences provides a first configuration sequence to direct a first configuration of the plurality of computational elements; and

wherein a second information sequence of the plurality of information sequences provides first operand data to the first configuration of the plurality of computational elements.

32. The module of claim 31, further comprising:

a third information sequence of the plurality of information sequences, the third information sequence providing routing information for the first information sequence and the second information sequence.

33. The module of claim 31, wherein the first information sequence is a configuration specification.

34. The module of claim 31, wherein the first information sequence is a reference to a stored configuration specification.

35. The module of claim 31, wherein the first information sequence and the second information sequence have a discrete, packet form.

36. The module of claim 31, wherein the first information sequence and the second information sequence have a continuous, stream form.

37. The module of claim 31, further comprising:

a fourth information sequence of the plurality of information sequences, the fourth information sequence providing power control for a selected computational element.

38. The module of claim 31, further comprising:

a fifth information sequence of the plurality of information sequences, the fifth information sequence providing instantiation duration control for a configuration of computational elements.

39. The module of claim 31, further comprising:

a sixth information sequence of the plurality of information sequences, the sixth information sequence providing security control for a configuration of computational elements.

40. A method for adaptive configuration and operation, the method comprising:

receiving a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

in response to the first configuration information, configuring through an interconnection network and providing the first operand data to a plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and

in response to the second configuration information, reconfiguring through the interconnection network and providing the second operand data to the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes, the first functional mode being different than the second functional mode.

41. The method of claim 40, wherein the first executable information module provides a first operating mode.

42. The method of claim 41, further comprising:

receiving a second executable information module, the second executable information module providing a second operating mode.

43. The method of claim 40, further comprising:

operating a first portion of the plurality of heterogeneous computational elements in the first functional mode while configuring a second portion of the plurality of heterogeneous computational elements for the second functional mode.

44. The method of claim 40, further comprising:

storing the first executable information module in a memory.

45. The method of claim 40, further comprising:

storing the first executable information module in a second plurality of heterogeneous computational units configured for a memory functional mode.

46. The method of claim 40, further comprising:

storing the first plurality of configuration information as a configuration of the plurality of heterogeneous computational units.

47. The method of claim 40, further comprising:

storing the first executable information module in a machine-readable medium.

48. The method of claim 40, wherein the first executable information module is received through an air interface.

49. The method of claim 40, wherein the first executable information module is received through a wireline interface.

50. The method of claim 40, wherein the first executable information module is embodied as a plurality of discrete information data packets.

51. The method of claim 40, wherein the first executable information module is embodied as a stream of information data bits.

52. The method of claim 40, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of specific architectures, the plurality of specific architectures including functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, routing, and field programmability.

53. The method of claim 40, wherein the plurality of functional modes includes linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

54. The method of claim 40, further comprising:

coordinating the configuration of the plurality of heterogeneous computational elements for the first functional mode with the first operand data and coordinating the reconfiguration of the plurality of heterogeneous computational elements for the second functional mode with the second operand data.

55. The method of claim 40, wherein the method is operable within a mobile station having a plurality of operating modes, the plurality of operating modes including mobile telecommunication, personal digital assistance, multimedia reception, mobile packet-based communication, and paging.

56. The method of claim 40, wherein the method is operable within a server having a plurality of operating modes.

57. The method of claim 40, wherein the method is operable within an adjunct network entity having a plurality of operating modes.

58. The method of claim 40, further comprising:

configuring the plurality of heterogeneous computational elements to generate a request for a second executable information module, the second executable information module providing a second operating mode.

59. The method of claim 40, wherein the method is operable within an integrated circuit.

60. The method of claim 40, wherein the first executable information module further comprises:

a first routing sequence coupled to the first configuration information to provide routing of the first configuration information within the interconnection network; and

a second routing sequence coupled to the second configuration information to provide routing of the second configuration information within the interconnection network.

61. The method of claim 40, wherein the first executable information module further comprises:

a power control sequence to direct the interconnection network to not provide a clock signal to a selected heterogeneous computational element of the plurality of heterogeneous computational elements.

62. The method of claim 40, wherein the first executable information module further comprises:

an iteration control sequence to direct a temporal continuation of a selected configuration of the plurality of heterogeneous computational elements.

63. The method of claim 40, wherein the first configuration information is a reference to a previously stored configuration sequence.

64. A method for adaptive configuration, the method comprising:

transmitting a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

wherein when a first executable information module is received, an interconnection network coupled to a plurality of heterogeneous computational elements is operative to configure and provide the first operand data to the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes, in response to the first configuration information, and the interconnection network further operative to reconfigure and provide the second operand data to the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes, in response to the second configuration information, the first functional mode being different than the second functional mode; and

wherein the plurality of heterogeneous computational elements include a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture.

65. The method of claim 64, wherein the first executable information module provides a first operating mode.

66. The method of claim 60, further comprising:

transmitting a second executable information module, the second executable information module providing a second operating mode.

67. The method of claim 64, further comprising:

accessing the first executable information module in a memory.

68. The method of claim 64, further comprising:

accessing the first executable information module in a second plurality of heterogeneous computational units configured for a memory functional mode.

69. The method of claim 64, further comprising:

accessing the first executable information module in a machine-readable medium.

70. The method of claim 64, wherein the first executable information module is transmitted through an air interface.

71. The method of claim 64, wherein the first executable information module is transmitted through a wireline interface.

72. The method of claim 64, wherein the first executable information module is embodied as a plurality of discrete information data packets.

73. The method of claim 64, wherein the first executable information module is embodied as a stream of information data bits.

74. The method of claim 64, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of specific architectures, the plurality of specific architectures including functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

75. The method of claim 64, wherein the plurality of functional modes includes linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations.

76. The method of claim 64, wherein the method is operable within a base station having a plurality of operating modes.

77. The method of claim 64, wherein the method is operable within a server having a plurality of operating modes.

78. The method of claim 64, wherein the method is operable within an adjunct network entity having a plurality of operating modes.

79. The method of claim 64, wherein the method is operable within an integrated circuit.

80. The method of claim 64, wherein the method is operable within a local area network.

81. The method of claim 64, wherein the method is operable within a wide area network.

82. The method of claim 64, wherein the method is operable within a wireline transmitter.

83. The method of claim 64, further comprising:

receiving a request for transmission of a second executable information module, the second executable information module providing a second operating mode.

84. The method of claim 64, wherein the first executable information module further comprises:

a first routing sequence coupled to the first configuration information to provide routing of the first configuration information within the interconnection network; and

a second routing sequence coupled to the second configuration information to provide routing of the second configuration information within the interconnection network.

85. The method of claim 64, wherein the first executable information module further comprises:

a power control sequence to direct the interconnection network to not provide a clock signal to a selected heterogeneous computational element of the plurality of heterogeneous computational elements.

86. The method of claim 64, wherein the first executable information module further comprises:

an iteration control sequence to direct a temporal continuation of a selected configuration of the plurality of heterogeneous computational elements.

87. The method of claim 64, wherein the first configuration information is a reference to a previously stored configuration sequence.

88. An adaptive integrated circuit, comprising:

configuration information and operand data;

a plurality of fixed and differing computational elements; and

an interconnection network coupled to the plurality of fixed and differing computational elements, the interconnection network operative in response to the configuration information to configure and reconfigure the plurality of fixed and differing computational elements for a plurality of functional modes.

89. The adaptive integrated circuit of claim 88, wherein the configuration information provides an operating mode for use of the operand data.

90. The adaptive integrated circuit of claim 88, wherein the plurality of functional modes includes linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

91. The adaptive integrated circuit of claim 88, wherein the configuration information is stored in a portion of the plurality of fixed and differing computational elements configured for a memory functional mode.

92. The adaptive integrated circuit of claim 88, wherein the configuration information is stored as a configuration of the plurality of fixed and differing computational elements.

93. The adaptive integrated circuit of claim 88, wherein the plurality of fixed and differing computational elements are selected from a plurality of specific architectures, the plurality of specific architectures including functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

94. The adaptive integrated circuit of claim 88, wherein the plurality of fixed and differing computational elements are configured to identify and select the configuration information from a singular bit stream containing the operand data commingled with the configuration information.

95. The adaptive integrated circuit of claim 88, further comprising:

a routing sequence coupled to the configuration information to provide routing of the configuration information within the interconnection network

96. The adaptive integrated circuit of claim 88, further comprising:

a power control sequence to direct the interconnection network to not provide a clock signal to a selected heterogeneous computational element of the plurality of heterogeneous computational elements.

97. The adaptive integrated circuit of claim 88, further comprising:

an iteration control sequence to direct a temporal continuation of a selected configuration of the plurality of heterogeneous computational elements.

98. The adaptive integrated circuit of claim 88, wherein the configuration information is a reference to a previously stored configuration sequence.

99. An adaptive integrated circuit, comprising:

a plurality of executable information modules, the plurality executable information modules including a first executable information module and a second executable information module, the first executable information module and the second executable information module each having corresponding operand data;

a plurality of reconfigurable matrices, the plurality of reconfigurable matrices including a plurality of heterogeneous computation units, each heterogeneous computation unit of the plurality of heterogeneous computation units formed from a selected configuration, of a plurality of configurations, of a plurality of fixed computational elements, the plurality of fixed computational elements including a first computational element having a first architecture and a second computational element having a second architecture, the first architecture distinct from the second architecture, the plurality of heterogeneous computation units coupled to an interconnect network and reconfigurable in response to the plurality of executable information modules; and

a matrix interconnection network coupled to the plurality of reconfigurable matrices, the matrix interconnection network operative to configure the plurality of reconfigurable matrices in response to the first executable information module for a first operating mode and to provide corresponding operand data to the plurality of reconfigurable matrices for the first operating mode, and to reconfigure the plurality of reconfigurable matrices in response to the second executable information module for a second operating mode and to provide corresponding operand data to the plurality of reconfigurable matrices for the second operating mode.

100. The adaptive integrated circuit of claim 99, further comprising:

a controller coupled to the plurality of reconfigurable matrices, the controller operative to provide the plurality of executable information modules to the reconfigurable matrices and to the matrix interconnection network.

101. A system for operating an adaptive and reconfigurable integrated circuit, the system comprising:

means for spatially configuring and reconfiguring a plurality of computational elements to form a first plurality of configured computational elements for the performance of a first plurality of selected functions;

means for temporally configuring the plurality of computational elements to form a second plurality of configured computational elements for the performance of a second plurality of selected functions;

means for providing data to the first and second pluralities of configured computational elements; and

means for coordinating the spatial and temporal configurations of the plurality of computational elements with the provision of the data to the first and second pluralities of configured computational elements.

102. An adaptive integrated circuit, comprising:

a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture;

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes, in response to the first configuration information, and to provide the first operand data to the plurality of heterogeneous computational elements for the first operating mode, and the interconnection network further operative to reconfigure the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes, in response to the second configuration information, the first functional mode being different than the second functional mode, and to provide the second operand data to the plurality of heterogeneous computational elements for the second operating mode;

wherein a first subset of the plurality of heterogeneous computational elements is configured for a controller operating mode, the controller operating mode including functions for directing configuration and reconfiguration of the plurality of heterogeneous computational elements, for selecting the first configuration information and the second configuration information from the first executable information module, and for coordinating the configuration and reconfiguration of the plurality of heterogeneous computational elements with respective first operand data and second operand data; and

wherein a second subset of the plurality of heterogeneous computational elements is configured for a memory operating mode for storing the first configuration information and the second configuration information.

103. An adaptive integrated circuit, comprising:

a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture of a plurality of fixed architectures, the first fixed architecture being different than the second fixed architecture, and the plurality of fixed architectures including functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes, in response to the first configuration information, the interconnection network further operative to reconfigure the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes, in response to the second configuration information, the first functional mode being different than the second functional mode, and the plurality of functional modes including linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations, and the interconnection network further operative to respectively provide first operand data and second operand data to the plurality of heterogeneous computational elements for the first functional mode and for the second functional mode.

104. An adaptive integrated circuit, comprising:

an executable information module, the module having first configuration information and second configuration information, the module further having operand data;

a plurality of fixed and differing computational elements; and

an interconnection network coupled to the plurality of fixed and differing computational elements, the interconnection network operative in response to the first configuration information to configure the plurality of fixed and differing computational elements to have an operating system, the operating system further operative to control, route and time reconfigurations of the plurality of fixed and differing computational elements for a plurality of functional modes in response to the second configuration information, the plurality of functional modes operative to utilize the operand data.

105. The adaptive integrated circuit of claim 104, wherein the operating system is further operative to generate third configuration information.